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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application of

Applicant	: Howard E. Rhodes and Luan Tran
Serial No	: 09/008,531
Filed	: January 16, 1998
Title	: **METHOD OF MAKING A SEMICONDUCTOR DEVICE HAVING IMPROVED CONTACTS**
Docket	: MIO 0012 V2 (94-0012.04)
Examiner	: M. Trinh
Art Unit	: 2822
Conf. No	: 6336

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Timothy W. Hagan
Attorney **Reg. No. 29,001**

Sir:

RESPONSE TO NOTIFICATION OF NON-COMPLIANCE with 37 CFR 1.192(c)

Pursuant to the Notification of Non-Compliance mailed July 23, 2004, enclosed is a complete new Brief on Appeal in triplicate in compliance with 37 CFR 1.192(c). The enclosed Brief now contains a correct copy of the appealed claims as an appendix thereto pursuant to 37 CFR 1.192(c)(9).

Please direct any questions or comments to the undersigned attorney.

Respectfully submitted,
DINSMORE & SHOHL LLP

By Timothy W. Hagan
Timothy W. Hagan
Registration No. 29,001

One Dayton Centre
One South Main Street, Suite 1300
Dayton, Ohio 45402-2023
(937) 449-6400
Facsimile: (937) 223-0724
E-mail: tim.hagan@dinslaw.com
TWH/amm

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BRIEF ON APPEAL

This is an appeal from the Office Action mailed October 22, 2003, finally rejecting claims 21-25, 31, and 32, all of the claims in the application. A Notice of Appeal was timely mailed on January 22, 2004, with the accompanying fee. Our check in the amount of $330.00 accompanies this Brief in accordance with 37 CFR §1.17(c). A request for a two-month extension of time in which to file this brief also accompanies this paper.

Real Party in Interest

The real party in interest in this application is Micron Technology, Inc., by an assignment from the named inventors recorded in the files of the U.S. Patent and Trademark Office.

Related Appeals and Interferences

Applicants know of no other related appeal or interference that will directly or indirectly affect or have a bearing on the outcome of this appeal.

Status of Claims

Claims 21-25, 31, and 32 are pending in this application and are before this Board for consideration on appeal. A copy of the appealed claims is found in the Appendix attached to this brief.

Status of Amendments

All of the amendments previously filed in this application have been entered.

Summary of the Invention

Applicants' invention is directed to a method of making a semiconductor device and in one embodiment includes forming a conductive layer having a topography that includes a substantially vertical component, forming an overlayer, etching a contact hole in the overlayer in an overetch amount into the substantially vertical component of the conductive layer, and forming a contact in the hole adjacent to and directly contacting the vertical component of the conductive layer.

As described in the specification at pages 2-3 and shown in Figs. 1, 2, 3A, and 3B, with prior art fabrication techniques, it was difficult to ensure that contact holes etched through an overlayer would stop precisely on the conductive layer to which the contact would be made. For example, as described at page 3, lines 17-34, and shown in Figs. 3A and 3B, a contact hole can be overetched into and sometimes through cell poly layer 2. Such a result diminishes the effectiveness of the contact by causing undesirable high resistance between conductor 16 and cell poly 2 (Fig. 3A) or may even cause electrical shorting (Fig. 3B).

In an embodiment of the present invention described at pages 8-11 and shown in Figs. 4-7, a substrate 22, 23, having at least one semiconductor layer is provided. An underlayer 20 having an opening 24 is formed over the semiconductor layer (page 8, lines 8-20). A layer of conductive material 26 is formed over the underlayer and into the opening (Fig. 5), the conductive material having a topography that includes a substantially vertical component in the opening. An overlayer 28 is then formed over the layer of conductive material. Referring to Fig. 6, and page 8, lines 21-32, a contact hole

30 is etched in the overlayer and in an overetch amount of the substantially vertical component of the layer of conductive material in the opening. As shown in Fig. 7, and described at page 9, lines 29-34 and page 10, lines 1-2, a contact 32 is then formed in the contact hole which is disposed adjacent to and directly contacting the vertical component of the conductive material.

Issues Presented

The issues presented for review on appeal are:

(1) Whether the Examiner erred in rejecting claims 21-24, and 31-32 under 35 USC §102(e) as being anticipated by Zamanian (U.S. 5,793,111);

(2) Whether the Examiner erred by rejecting claims 21-25, and 31-32 under 35 USC §103(a) as being unpatentable over Matsuo et al (U.S. 5,312,769) taken with Zamanian and Toshiyuki et al (JP-05-109905);

(3) Whether the Examiner erred in rejecting claims 21-25 and 31-32 under 35 USC §103(a) as being unpatentable over Okada et al (U.S. 5,399,890) taken with Zamanian and Toshiyuki et al; and

(4) Whether the Examiner carried his burden of establishing a prima facie case for the unpatentability of any claim on appeal.

Grouping of Claims

The Examiner has stated three grounds of rejection, namely: (1) claims 21-24, and 31-32 under 35 USC §102(e) as being anticipated by Zamanian; (2) claims 21-25, and 31-32 under 35 USC §103(a) as being unpatentable over Matsuo et al taken with Zamanian and Toshiyuki et al; and (3) claims 21-25 and 31-32 under 35 USC §103(a) as being unpatentable over Okada et al taken with Zamanian and Toshiyuki et al.

This application contains two independent claims, claims 21 and 31. Applicants will separately argue the patentability of additional dependent claims in the body of their argument section.

References

Zamanian, U.S. Patent No. 5,793,111

Zamanian teaches a semiconductor integrated circuit having an improved landing pad. Referring to Fig. 6, Zamanian teaches an oxide layer 28 that includes an opening 30 (see Fig. 2) formed through the oxide layer 28. A polysilicon layer 32 is formed over the oxide layer 28 and the contact opening 30. A silicide layer 36 is formed over the polysilicon layer 32. A barrier layer 34 is formed over the silicide layer 36. A dielectric layer 40, contact opening 42, and conductive contact 44 are formed, wherein barrier layer 34 is located in the bottom of the contact opening underlying the aluminum contact layer 44. See col. 5 lines 49-63.

Matsuo et al, U.S. Patent No. 5,312,769

Matsuo et al. teaches a p-type silicon substrate having a n+-type diffused region formed in the silicon substrate 1, a gate oxide film 4 formed on the silicon substrate, an insulating film 21, and a first interlayer insulating film 23 formed on the insulating film 21 covering first and second polycrystalline silicon lead pads 12 and 22. The first interlayer insulating film 23 is not overetched when forming the contact hole.

Toshiyuki et al, Japanese Patent JP-05-109905

Toshiyuki et al. teach etching of an insulating layer 3 to form an opening in the contact layer 2 and filling this contact layer 2 with an electrode layer 6.

Okada et al, U.S. Patent No. 5,399,890

Okada et al. teach a semiconductor memory that includes an isolation region 2 and transistors 3a and 3b formed on a semiconductor substrate 1. A bit line 4 of a metal or silicide or polycide is formed on the semiconductor substrate on which a first interlayer insulating film 5 is deposited. Contact holes 6 and 6a are formed after which a conductive layer is formed. The conductive layer is patterned to form node electrode 7a and a first level interconnection layer 7b. A capacitance insulating film 8 is then formed over the node electrode 7a and the first level interconnection layer 7b. The capacitance

insulating film 8 is etched to form a plate electrode 9. A second interlayer insulating film 10, formed of silicon oxide, is formed over the plate electrode 9. Contact holes 11 that reach designated regions of the plate electrode 9 and the first level interconnection layer 7b are opened through the second interlayer insulating film 10.

ARGUMENT

A. Zamanian does not anticipate any of the claims.

In the final rejection (Paper No. 35), the Examiner rejected claims 21-24 and 31-32 under 35 USC §102(e) as anticipated by Zamanian. Zamanian teaches a semiconductor integrated circuit having an improved landing pad. Referring to Fig. 6, Zamanian teaches an oxide layer 28 that includes an opening 30 (see Figs. 2 and 3) formed through the oxide layer 28. A polysilicon layer 32 is formed over the oxide layer 28 and the contact opening 30. A silicide layer 36 is formed over the polysilicon layer 32. A barrier layer 34 is formed over the silicide layer 36. A dielectric layer 40, contact opening 42, and conductive contact 44 are formed, wherein barrier layer 34 is located in the bottom of the contact opening underlying the aluminum contact layer 44. See col. 5, lines 49-63.

To determine whether Zamanian anticipates the claims, one must first properly construe those claims and the terminology used therein. Then one must carefully compare what Zamanian actually describes (versus what the Examiner contends it describes) to the claim language. When that analysis is correctly performed, the conclusion is inescapable that Zamanian does not teach or suggest each and every element of the claims.

As understood, the Examiner relied on only the Fig. 6 embodiment of Zamanian in the final rejection. Claim 21 recites that the layer of conductive material is formed **in** the opening of the underlayer and that the contact hole is etched in the overlayer and in an overetch amount of the substantially vertical component of the layer of conductive material **in the opening**. This feature of the claimed invention is found in the specification with reference to the embodiment shown in Figs. 6 and 7, and described beginning at page 8, line 21, and continuing onto page 10. By "opening," applicants

intend that term to have a meaning as one of ordinary skill in the art would understand that term's meaning. Specifically, in the context of the presently-claimed invention, the "opening" is "an open space serving as a passage or gap," and "a hole or aperture." *The American Heritage Dictionary of the English Language* (1978).

The only "opening over the at least one semiconductor layer" shown in Zamanian is the opening formed in dielectric layer 28 that is formed by etching. "As shown in FIG. 2, contact opening 30 is formed through dielectric layer 28, for example by way of reactive ion etching or another type of anisotropic etching." See, col. 4, lines 18-20.

What Zamanian forms in contact opening 30 is polysilicon layer 32. See, col. 4, lines 36-38 ("polysilicon layer 32 is formed ... in the contact opening 30"). Claim 21 recites "forming an underlayer having an opening" and "forming a layer of conductive material over the underlayer and in said opening." Thus, what Zamanian explicitly describes is the formation of a dielectric layer 28 having an opening 30, and then forming a polysilicon layer (which is a conductive material) in that opening. However, if polysilicon layer 32 is the "layer of conductive material," then it is not etched at all during formation of the contact hole and cannot meet the other language recited in claim 21, and dependent claims 22-24 ("etching a contact hole in said overlayer and in an overetch amount of the substantially vertical component of said layer of conductive material in said opening"). Thus, the structure and method of forming it that is explicitly described in Zamanian does not meet each and every limitation of independent claim 21 and claims 22-25 which depend therefrom.

What the Examiner has asserted in the final rejection, however, is not a process that Zamanian explicitly teaches. Rather, the Examiner has asserted that other layers that are formed during Zamanian's process correspond to the claimed invention. Applicants will demonstrate that Zamanian does not fairly teach or suggest the claimed method. As understood, the Examiner asserted that barrier layer 34 corresponds to the claimed layer of conductive material ("the layer of conductive material 34;" final rejection, page 2), and that Zamanian describes in column 6 that a portion of barrier layer 34 may be etched away during formation of the contact opening.

However, if barrier layer 34 is the "layer of conductive material," then it does not have a substantially vertical component "in said opening" as recited in claim 21. As discussed above, Zamanian states that polysilicon layer 32 occupies what was opening 30 (Figs. 2 and 3). Thus, the poly layer 32, not the barrier layer 34, is located in opening 30.

As clearly shown in Fig. 6 of Zamanian, the figure that the Examiner relies upon to make the rejection, barrier layer 34 does not extend into opening 30. Rather, barrier layer 34 lies atop layers 36 and 32 which the Examiner characterizes as "an underlayer structure." But, if layers 36 and 32 form an "underlayer structure," there is no opening in such structure because layers 36 and 32 are clearly shown in Fig. 6 as being continuous (i.e., there are no apertures or gaps). The only layer having an opening and which is in the correct position in the Zamanian structure is dielectric layer 28 (a layer the Examiner ignores in making the rejection). Because layers 36 and 32 have no "opening" in accordance with the commonly-understood meaning of that term, Zamanian does not teach each and every element of the claimed invention and cannot anticipate claim 21, and claims 22-24 which depend therefrom.

With respect to dependent claim 23, that claim recites that the vertical component of the conductive material is a spacer. This embodiment of the invention is shown in Figs. 8-10 where the vertical component of the localized thick region of the conductive layer is formed along sidewalls 36 of underlayer 20. While the Examiner asserted in the final rejection that Zamanian shows a layer of conductive material having the vertical component formed as a spacer, applicants disagree. As understood, the Examiner asserted that barrier layer 34 of Zamanian corresponded to the claimed layer of conductive material (final rejection, page 2). Barrier layer 34 does not comprise a spacer; rather, as clearly shown in Fig. 6 it forms a layer over silicide layer 36. The only spacer structure shown by Zamanian are spacers 18. Claim 23 is patentable for this additional reason.

With respect to claim 24, that claim recites that the process comprises the further step of forming a structure having an opening therein under the conductive layer and filling the opening with "said conductive material" to form the vertical component of the layer of conductive material. The Examiner asserted in the final rejection that Zamanian

forms a structure 28 ("oxide layer 28") having an opening therein and fills that opening "with the conductive material to form the vertical component." Again, as understood, the Examiner asserted that barrier layer 34 corresponded to the conductive layer. As such, Zamanian's barrier layer 34 does not "fill the opening with said conductive material" as claimed in claim 24. Rather, as explicitly taught by Zamanian, it is polysilicon layer 32 that fills the opening in oxide layer 28. For this additional reason, claim 24 is patentable over Zamanian.

Independent claim 31 recites that the contact hole is formed in the overlayer and in the vertical component of the layer of conductive material in the opening. Claim 31 also recites that the contact hole is disposed adjacent to and directly contacts the vertical component of the conductive material in the opening. Again, this feature of the invention is described in the specification with reference to Figs. 6 and 7, beginning at page 8, line 21, and continuing onto page 10.

Zamanian's barrier layer 34 in the Fig. 6 embodiment, and asserted to correspond to the claimed "conductive layer," does not fill the opening as recited. As explicitly taught by Zamanian, poly layer 32 occupies what was opening 30. If polysilicon layer 32 is considered to be the "conductive material," then no portion of the contact hole is formed in layer 32, and the contact hole does not directly contact that layer as recited in claim 31. For all of these reasons, Zamanian does not anticipate claim 31 because Zamanian does not show each and every element of the claimed invention. Thus, applicants submit that claim 31, and claim 32 which depends therefrom, are not anticipated by Zamanian.

B. The Claims would not have been obvious over Matsuo.

In the final rejection, the Examiner rejected claims 21-25 and 31-32 under 35 USC §103 as unpatentable over Matsuo et al taken with Zamanian and Toshiyuki. The Examiner's explanation of his assertions concerning Matsuo's teachings was confusing at best. For example, in lines 10-11 of the paragraph numbered 2. on page 3 of the final rejection, the Examiner asserted that Matsuo taught an overetching step, while in a later paragraph on the same page, the Examiner conceded that Matsuo did not teach such a

step. Further, the Examiner mixed up different embodiments of Matsuo, incorrectly referring to "contact hole window 29" as being associated with the Fig. 2A-2E embodiment when in fact that feature is shown in Fig. 3A. Applicants will respond to the rejection and reasoning as best understood.

Matsuo teaches forming transistors on a semiconductor substrate, and then forming polysilicon lead pads that are electrically connected to the transistors. An interlayer insulating film is formed over the transistors and lead pads. Bit lines are then electrically connected to the transistors and a second interlayer insulating film is formed over the bit lines. Contacts holes are formed in the first interlayer insulating film to expose the lead pads. Polysilicon is then selectively grown on the surfaces of the exposed lead pads.

With respect to claim 21, that claim recites "forming an underlayer having an opening over the at least one semiconductor layer." Matsuo, to the contrary, describes word lines 102-104 having an insulating film 21 "formed around the word lines" (col. 4, lines 13-14). The Examiner asserted that insulating film 21 corresponded to the claimed underlayer. However, as shown in the figures, there is no "opening" in any of the insulating films 21. Such films form a continuous structure "around the word lines." If the Examiner is pointing to the areas *between* the word lines 102-104, then that structure fails to describe an underlayer having an opening in the underlayer. For these reasons, neither Matsuo, nor the secondary references, teach or suggest this claim limitation.

Additionally, the Examiner appears to have conceded (see above) that "Matsuo fails to show etching in an overetch amount of the substantially vertical component" (final rejection, page 3). The Examiner attempted to remedy this admitted deficiency in Matsuo by turning to Zamanian and Toshiyuki. However, as discussed above, Zamanian's conductive layer 32 of polysilicon is not etched at all. It is the barrier layer 34 that is etched. The teachings of Matsuo and Zamanian are not combinable in the manner proposed by the Examiner. Matsuo does not need a multi-layer "pad" that includes a barrier layer. And Zamanian fails to teach overetching of a conductive layer.

Toshiyuki shows a very different geometry for the formation of an interconnect structure. There is no motivation to use the technique of Toshiyuki to expose the very

different polysilicon lead pads of Matsuo. The Examiner has failed to carry his burden of establishing, by evidence, a prima facie case for obviousness.

With respect to claim 31, as discussed above, no portion of Zamanian's conductive layer 32 has a contact hole etched therein. Nor does Toshiyuki teach or suggest a contact hole in an overlayer that extends into the vertical component of a layer of conductive material. The Examiner concedes that Matsuo also does not. Thus none of the cited references, either taken alone or together teach or suggest the claimed subject matter of claims 31-32. For all of these reasons, applicant submits that claims 21-25 and 31-32 as amended are patentable over Matsuo, Zamanian, and Toshiyuki.

C. **The Claims would not have been obvious over Okada.**

In the final rejection, the Examiner rejected claims 21-25 and 31-32 under 35 USC §103 as unpatentable over Okada taken with Zamanian and Toshiyuki. Okada does not teach forming a structure having an opening in a semiconductor layer and filling the opening with a layer of conductive material. The Examiner has combined unrelated bits and pieces of disclosure from multiple embodiments of Okada to arrive at his conclusions. Okada explicitly describes separate embodiments of the invention, namely, Figs. 2A-2C ("first example"), Fig. 3 ("second example"), and Figs. 5 and 6A-6D ("third example"). That Okada may perform different steps and form different structures in different embodiments of the invention does not teach or suggest applicants' claimed process. For example, elements 7a and 7b of Okada cannot be both "an underlayer structure 7a/7b,8 having and opening (Fig 5)" and "the at least one semiconductor layer 7a/7b" (see final rejection, page 5, lines 1-2). Further the Examiner has not carried his burden of specificity in explaining the rejection by simply asserting that there is an "opening" somewhere in the Fig. 5 embodiment ("having an opening (Fig 5)").

The layer of conductive material 9 in Okada's Figs. 2A-C simply lies upon the semiconductor structure. Contact holes 6 and 6a are filled by electrode material 7a and 7b. An insulating film 8 then overlies the electrodes. Conductive layer 9 is deposited over film 8. No "openings" in film 8, which the Examiner asserts to be part of the "underlayer" taught by Okada, are filled with any conductive material 9. Further,

contacts 12 extend only to the surface of conductive layer 9 and do not extend into any vertical component of the conductive layer 9 as recited in claim 31. Thus, even if the reference teachings were to be combined in the manner proposed by the Examiner, the claimed invention would not result.

Further, one skilled in the art would not combine the teachings of Zamanian and Toshiyuki with Okada because Toshiyuki teaches away from the methods taught by Zamanian and Okada. As discussed above, Zamanian's conductive layer 32 of polysilicon is not etched at all. It is the barrier layer 34 that is etched. The teachings of Okada and Zamanian are not combinable in the manner proposed by the Examiner. Okada does not need a multi-layer "pad" that includes a barrier layer. And Zamanian fails to teach overetching of a conductive layer.

Toshiyuki shows a very different geometry for the formation of an interconnect structure. There is no motivation to use the technique of Toshiyuki to expose the very different conductive layers 9, 9A, and 9B of Okada. The Examiner has failed to carry his burden of establishing, by evidence, a prima facie case for obviousness against any of the claims.

For all of these reasons, applicants submit that claims 21-25 and 31-32 are patentable over the cited and applied references. This Board is requested to reverse all of the rejections made by the Examiner in their entirety.

Respectfully submitted,
DINSMORE & SHOHL LLP

By _____
Timothy W. Hagan
Registration No. 29,001

One Dayton Centre
One South Main Street, Suite 1300
Dayton, Ohio 45402-2023
(937) 449-6400
Facsimile: (937) 449-6405
E-mail: tim.hagan@dinslaw.com
TWH/

APPENDIX

Claims on Appeal

21. A process for making a semiconductor device comprising the steps of:

providing a substrate having at least one semiconductor layer;

forming an underlayer having an opening over the at least one semiconductor layer;

forming a layer of conductive material over the underlayer and in said opening, said layer of conductive material having a topography that includes a substantially vertical component in said opening;

forming an overlayer over the said layer of conductive material;

etching a contact hole in said overlayer and in an overetch amount of the substantially vertical component of said layer of conductive material in said opening; and

forming a contact in said contact hole disposed adjacent to and directly contacting said vertical component.

22. A process as claimed in claim 21 wherein said vertical component defines a localized thick region in the layer of conductive material.

23. A process as claimed in claim 21 wherein said vertical component is a spacer.

24. A process as claimed in claim 21 further comprising the step of forming a structure having an opening therein under said conductive layer and filling said opening with said conductive material to form said vertical component.

25. A process as claimed in claim 21 wherein said conductive layer is a capacitor electrode.

31. A process for making a semiconductor device comprising:

providing a substrate having at least one semiconductor layer;

forming a structure having an opening in said at least one semiconductor layer;

forming a layer of conductive material over said at least one semiconductor layer;

filling said opening with said conductive material to form a substantially vertical component in said opening;

forming an overlayer over said layer of conductive material;

forming a contact hole in said overlayer and extending into said vertical component of said layer of conductive material, said contact hole disposed adjacent to and directly contacting said vertical component in said opening; and

filling said contact hole with a conducting material.

32. A process as claimed in claim 31 wherein said vertical component defines a localized thick region in the layer of conductive material.